REMARKS

Pending Claims

Claims 12-26 are currently pending. Claims 12, 13, and 15 are currently amended. Claims 1-11 were previously canceled. No new matter is added.

Rejections Under 35 U.S.C. § 103

Claims 12-16 and 24-26 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of what the Examiner has termed the Applicant Admitted Prior Art ("AAPA") in view of Miyashita et al. (USP 5,610,954). In addition, claims 19-22 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA in view of Miyashita et al. further in view of Yonekura et al. (USP 5,761,617). Further, claims 17-18 stand rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA in view of Miyashita et al. further in view of Anumula et al. (USP 6,566,967). Finally, claim 23 stands rejected under 35 U.S.C. § 103(a) as being obvious over the combination of the AAPA, Miyashita et al., Anumula et al. and further in view of Yonekura et al. However, in view of the amendments and the arguments presented herein, Applicant respectfully submits that the rejections have been traversed and request that the rejections be reconsidered and withdrawn.

The combinations of references cited by the Examiner fail to render the claims obvious because none of the combinations of references teaches or suggests all of the elements of the claimed combinations. Among other distinctions, the AAPA does not teach or suggest, nor does Miyashita et al. supply the deficiencies of, a clock and data recovery circuit which includes two feedback loops in which the discriminator circuit is part of one of the loops and is in a separate feedback loop from the oscillator.

In the clock and data recovery circuit of claim 12, the first feedback loop is directed to "performing phase-synchronization of a recovered clock signal, output from said oscillator, with an input data signal" and the second feedback loop includes "a discriminator circuit … for discriminating said input data signal and outputting the discriminated signal."

The clock and data recovery circuit of claim 13 includes a first feedback loop with a first phase detector circuit for detecting the phase difference between a recovered clock signal and a received data signal and a second feedback loop including a discriminator circuit supplied with said received data signal a second phase detector circuit for detecting the phase difference

between an output data signal, discriminated and output by said discriminator circuit, and said received data signal. The clock and data recovery circuit of claim 15 includes a first feedback loop including a first phase detector circuit for detecting the phase difference between an input reference clock signal and a recovered clock signal and a second feedback loop including a discriminator circuit supplied with a received data signal and a second phase detector circuit for detecting the phase difference between an output data signal discriminated and output by said discriminator circuit and said received data signal. In the first feedback loop of the circuits of claims 13 and 15, the output of the phase detector is integrated and the integrated signal is provided as an input to an oscillator, separate from the discriminator circuit in the second feedback loop.

In the AAPA, namely Figure 11 of the present application, the discriminator 904 is not part of a feedback loop but instead has two inputs, "data in" and "clock out," and produces the "data out" signal, and therefore does not teach or suggest the discriminator circuit being part of a feedback loop. The circuit of Figure 7 of Miyashita et al., on the other hand, has a single feedback loop which includes both the discriminator and the oscillator. As noted in the present application, "the first feedback loop 204 for controlling the oscillation frequency of the VCO 203 and the second feedback loop 207 for data recovery are disunited [from] each other, so that the oscillation frequency and the phase of the VCO 203 may be controlled independently of each other." See p. 26, line 24 through p. 27 line 3 of the originally-filed specification. Further, the input data signal is compared with the discriminated signal in the second feedback loop and the phase between the two is automatically adjusted, separate from the adjustments to the oscillation frequency in the first feedback loop. See p. 15, lines 7-12 of the originally-filed specification.

Thus the combination of the AAPA in view of Miyashita et al. fails to render obvious any of independent claims 12, 13, or 15.

For at least the reason that each depends from an allowable independent claim and because each recites patentable subject matter, dependent claims 14 and 16-26 are also patentable.

CONCLUSION

In view of the remarks and amendments presented herein, reconsideration and withdrawal of the pending rejections and allowance of the claims are respectfully requested. The Examiner is strongly encouraged to contact the undersigned at the phone number below should any issues remain with respect to the application.

Respectfully submitted,

MICHAEL BEST & FRIEDRICH LLP

/thomas j. keating/

By: _____

Thomas J. Keating, Reg. No. 59,110
Tel.: 608-257-3501

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Michael Best & Friedrich LLP
Two Prudential Plaza
180 North Stetson Avenue, Suite 2000
Chicago, Illinois 60601
312.222.0800